

Responsive Processor for Parallel/Distributed Real-Time Processing

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Applications:

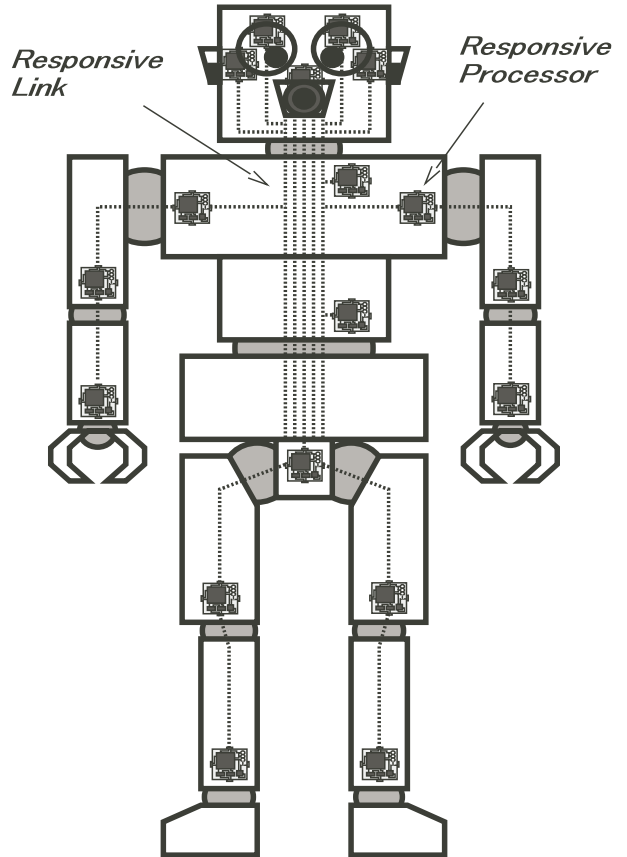
Robots, Office Automation, Factory Automation,
Home Automation, Intelligent Buildings, Amusement
Systems, ...

System-on-a-chip for Parallel/Distributed Real-time Control including:

- Processing Core (SPARC)
- **Responsive Link** (Real-Time Communication, 4 links/chip)
- I/O for Computer (SDRAM I/F, DMAC, PCI, USB, PIO, SIO, Timers, Counters, ...)
- I/O for Control (ADC, DAC, PWM Generators, Pulse Counters, ...)

Characteristics of Responsive Link:

- Split transmission of data and events
- Independent routing of data and events
- Forward error correction
- Fixed packet size: 64B data, 16B event
- Point-to-point
- Cut through switch with overtaking function
- Higher prioritized packet can overtake lower prioritized packet at each node.
- Flexible linkspeed(100Mbaud, 50Mbaud, 25Mbaud, 12.5Mbaud)
- Topology free



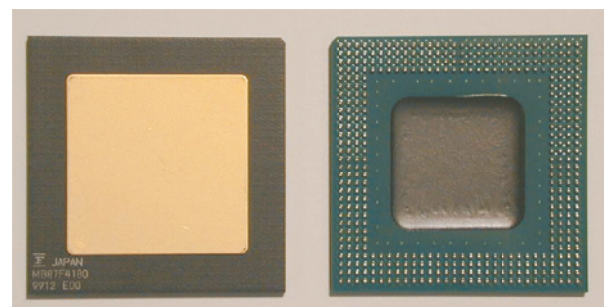
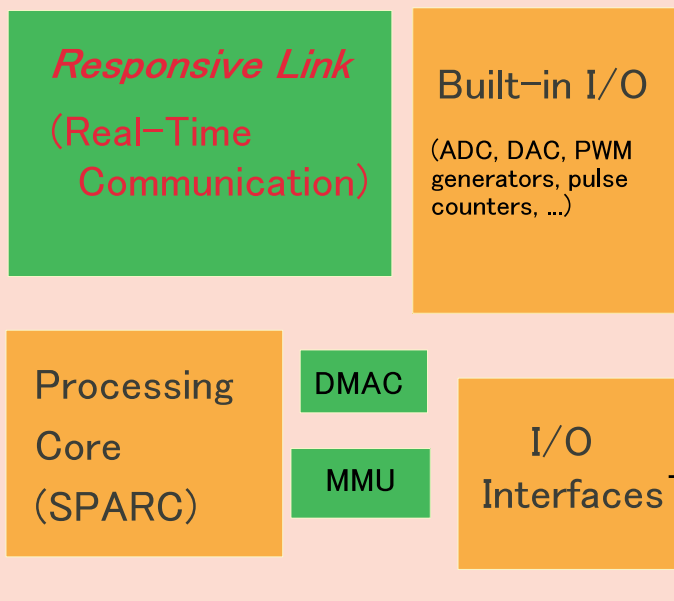
Performance of MPU

Clock(MHz)	100	80	60	40	20	Sleep
Speed(MIPS)	121	97	73	48	24	0
Power(W)	1.0	0.8	0.6	0.4	0.2	0.01

Performance of *Responsive Link*

Clock (MHz)	200	100	50	25
Max. Speed (Mbaud)	100	50	25	12.5
Speed of Data (Mbps)	67	33	17	8
Latency of Event(μ sec)	3.1	6.2	12.5	25
Power (W)	0.2	0.1	0.05	0.02

Responsive Processor



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