RMT Processor for Distributed Real-Time Control

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RMTP : Responsive MultiThreaded Processor

- Guarantee of processing time and communication time by hardware
- System-on-chip integrating all required functions for distributed real-time control

1. Multithreaded processing core for real-time processing: *RMT PU*
2. Real-time communication: *Responsive Link*
3. Computer I/Os: PCI-X, IEEE1394, DDR SDRAM I/Fs (128/32bit), Ethernet, 32bit DMAC (12ch), etc.
4. Control I/Os: PWM output x 6, PWM input x 3, pulse counter (A,B,Z) x 3, SPI (3cs x 2ch), digital I/O

- Low power consumption method: Dynamic Voltage and Frequency Scaling (DVFS) at each IP block
  Compound design by using low power highVt cells and high performance lowVt cells

RMT Processing Unit (RMT PU) :

Real-time processing by hardware
Context switching by software is converted to *RMT* executin (prioritized SMT execution) by hardware.

1. Prioritized simultaneous multithreading
   a. 8-thread simultaneous execution
   b. Context cache (32threads)
   c. 256 priority levels
   d. Waking up a thread by an interruption (Event-driven programming)
2. High performance vector units
   a. Flexible 2D vector units (FP, Int)
   b. Vector registers shared by multiple threads
3. Performance@100MHz

a. Context switch:	4clock cycle
b. Scalar Integer	400MIPS
c. Scalar Floating Point	200MFLOPS
d. Vector Integer (32bit)	3.2GIPS
e. Vector Integer (16bit)	6.4GIPS
f. Vector Integer (8bit)	12.8GIPS
g. Vector Floating Point(64bit)	1.6GFLOPS
h. Vector Floating Point(32bit)	3.2GFLOPS

Performance:0.1～2 times faster than Pentium4
Power consumption:1/100～1/20 (0.1～4W)

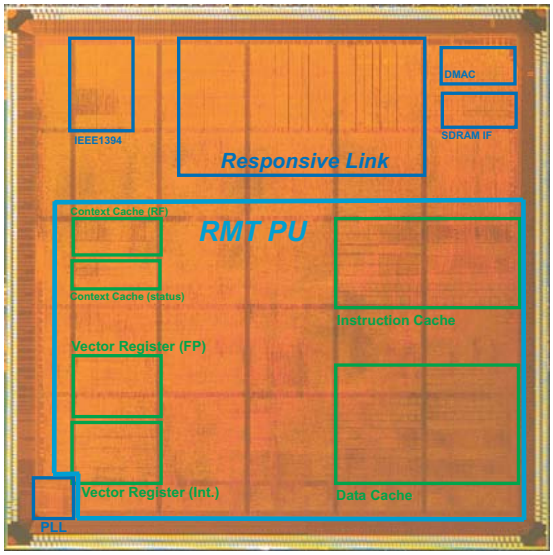


Fig.1 Photo of *μRMT Processor*

M-RMT Processor design process

1. Fabrication maker:TSMC
2. Process rule: 130nm CMOS
   8-layered Cu wiring
3. # of gates: 14M
4. Voltage:
   Core: 1.0V
   Memory: 2.5V
   I/O: 3.3V
5. Power: 0.1～4W
6. Die size: 10.0mm x 10.0mm

Responsive Link :

1. Real-time communication by hardware
   a. Hard real-time communication:Event link
   b. Soft real-time communication:Data link
   c. Cut-through switch with packet overtaking
   d. Independent routing of data and event links
   e. Priority replacement at each node
   f. 256 level priority
   g. 5 x 5 (5input 5output) router switch
2. Standardization
   a. International standard: ISO/IEC 24740:2008
   b. IPSJ-TS 0006:2003
3. Performance

a. Serial Link:	Parallel Link:
1way: 400 (Mbps/link)	1way: 1.6 (Gbps/link)
1pair:1.6 (Gbps/link)	1pair:6.4 (Gbps/link)

   b. Low latency (one-tenth of Gigabit Ethernet)

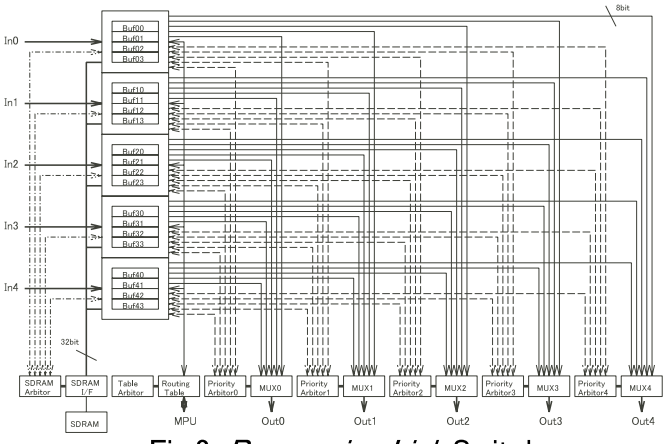


Fig.2. *Responsive Link* Switch with Packet Overtaking Function

RMT Processor families

- *RMT Processor* for distributed real-time processing
  TSMC 0.13um LV-FSG
- *μ RMT Processor* for humanoid robot control
  TSMC 0.13um LVHP
- *M-RMT Processor* for robot motion control
  TSMC 0.13um LVHP + LVHP HighVt
- HP-*RMT Processor* for video processing and planning of a humanoid robot
  TSMC 90nm LowK, Dual core

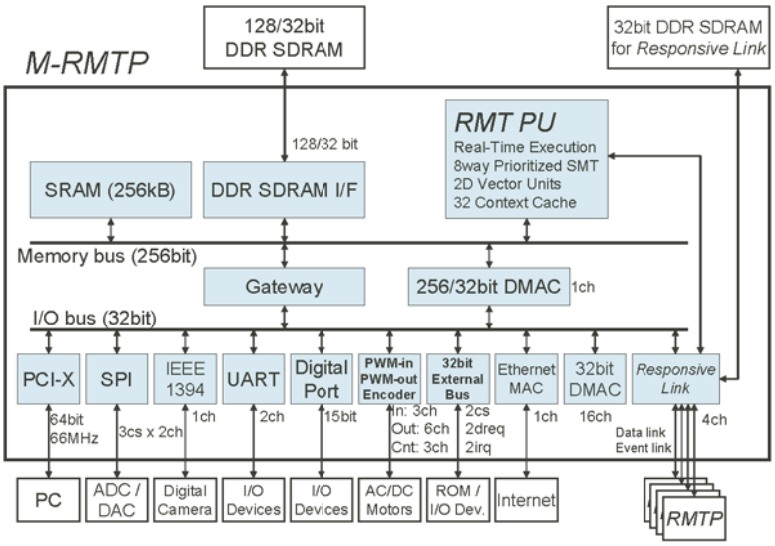


Fig. 3 Block Diagram of *M-RMTP*

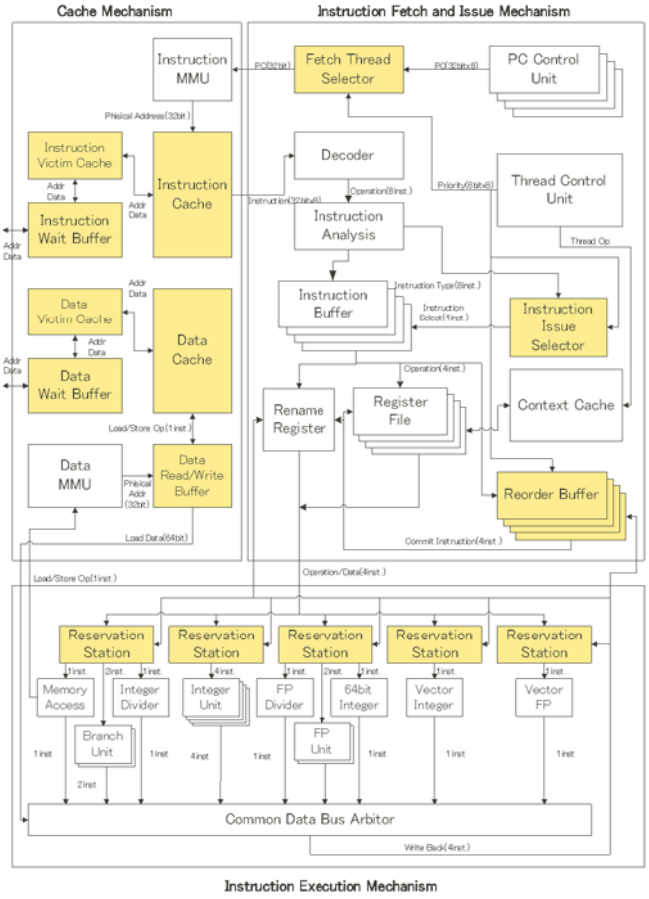


Fig. 4 Block Diagram of *RMT PU*

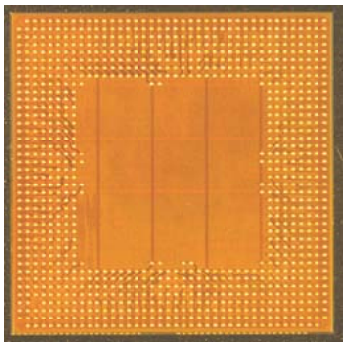


Fig. 4 Photo of Bare Dire of *M-RMTP*

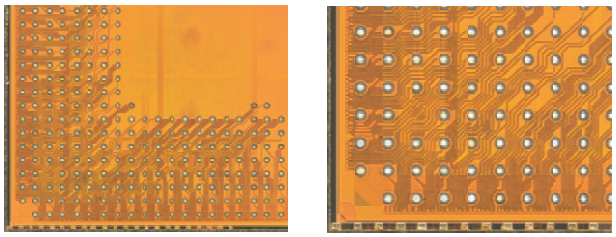


Fig. 5 Flip Chip Implementation

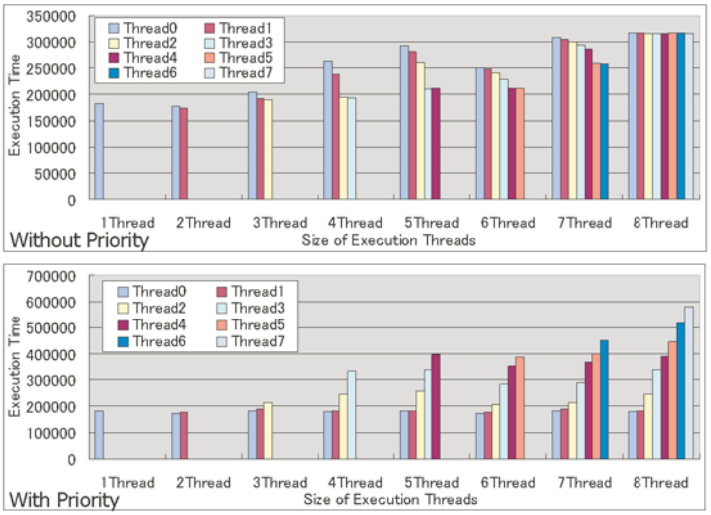
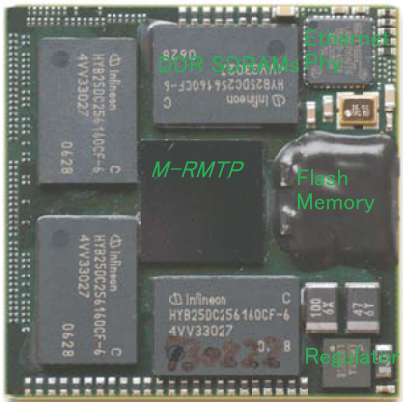


Fig.7 Execution w/wo Priority on *RMT Processor*



- DDR SDRAM x 4
- Termination Regulator for DDR SDRAM
- Flash Memory x 2
- Ethernet PHY
- Registers
- Capacitors
- Size: 33.0 x 33.0 mm

Fig. 6 *M-RMTP* SiP (System-in-Package)

No real-time scheduler is needed by using static scheduling up to 8 threads.

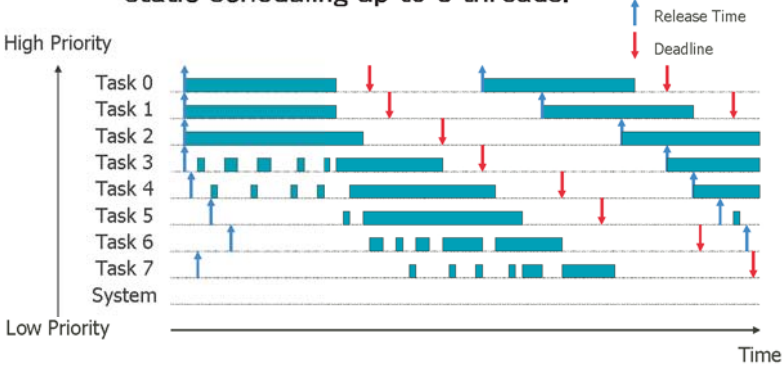


Fig.8 Real-Time Execution on *RMT Processor*